REMARKS

This is in response to the Office Action mailed on March 27, 2003 in which claims 1-7 were pending. Claim 1 was withdrawn from consideration. In the Office Action, claims 6 and 7 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 2-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over the Applicant's admitted prior art in view of Chang et al., U.S. Pat. No. 5,753,529 ("the Chang patent"). With this amendment, claim 7 is canceled without prejudice, claims 2-6 are amended, and new claims 8-14 are added. All of pending claims 1-6 and 8-14 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested.

Claims 6 and 7 were rejected under §112 as being indefinite. With this amendment, claim 7 is canceled without prejudice, and the element of claim 7 is added to claim 6 to clarify the low temperature element. Further, the explicit lines within claim 6 indicated by the Examiner have been amended to clarify the claim language. With this amendment, the rejection of claim 6 under §112 is overcome and should be withdrawn. Reconsideration and notice to that effect is respectfully requested.

With respect to the rejection of claims 2-7, the Office Action misstates the teachings of the admitted prior art. The Office Action states:

> "AAPA discloses a method for fabricating low-power-loss power semiconductor switching devices wherein the fabrication is in the following sequence (See Background of the Invention on page 1-4 of this application):
>
> fabricating a nonuniformly doped n-type substrate which contains a diffused n+ layer on one side, wherein the diffused layer, which is finally near to the backside p+ emitter, is formed in the first step of this procedure before the thinning of the substrate (page 1, line 18 to page 2, line 26);
>
> fabricating the general frontside structure of an IGBT (page 2, lines 2-3) on the low-concentration side of the n-type substrate using ion implanting, high-temperature diffusion (page 3, lines 16-17); and
>
> forming the backside p+ emitter with a required thickness by ion implanting into the surface of the diffused-layer (page 2, lines 5-6 and page 3, lines 18-19);
>
> AAPA fails to explicitly disclose thinning the wafer from the high-concentration side of the substrate by grinding and polishing so that the

thickness of the residual diffused-layer is decreased to a required value as recited in present claim 6."

See Office Action, p. 4. However, the admitted prior art described in the "Background of the Invention" on pages 1-4 of this application does not disclose a method in the sequence as stated by the Office Action.

The Application describes the PT-IGBT and NPT-IGBT. Both types of IGBT are **not** fabricated on a "nonuniformly doped n-type substrate which contains a diffused n^+ layer on one side" as asserted by the Examiner. For PT-IGBTs, the starting wafer is a *uniformly-doped* p^+ monocrystalline substrate. On this substrate, an n-type buffer layer and an n^- base layer are formed by means of epitaxy. Even if a person may view the $p/n/n^-$ structure as a whole substrate, he still cannot get a "nonuniformly doped n-type substrate". For NPT-IGBTs, the starting substrate is a *uniformly-doped* monocrystalline (normally FZ) n^- wafer. In this substrate structure (on the bottom or backside part of the wafer), the diffused n^+ layer never emerges throughout the fabrication process.

Additionally, the Application at page 2, lines 2-3 describes the formation of the frontside structure of an NPT-IGBT, which the text at page 3, lines 16-17 describes the formation of the frontside structure of an FS IGBT (Field Stop IGBT). Although the name FS IGBT is not mentioned explicitly in the application, the name is denominated by the authors of the article in ISPSD'2000, pp. 361-364, which is referenced at page 3, line 15 of the application. Both processes, however, are carried out on a *uniformly doped* n^- substrate, which is different from the present invention, where the substrate is of a **nonuniformly-doped** n-type.

The application at page 2, lines 5-6 describes the formation of the backside p^+ emitter of an NPT-IGBT, while the text at page 3, line 18-19 describes the formation of the backside p^+ emitter of an FS IGBT. Both processes, however, are not carried out on the surface of a diffused-layer. For NPT-IGBTs, the backside p^+ implanting is on the backside surface of a uniformly-doped monocrystalline n^- substrate. For this reason, the instant invention is allowable over the Applicant Admitted Prior Art and the cited art. Reconsideration and notice to that effect is respectfully requested.

Nevertheless, as mentioned in the application and the literature in PROC. ISPSD'2000, pp. 361-364, this n-type buffer layer is formed by implanting just before the p^+ implanting. It is not formed by diffusion, and moreover is not formed by a prior diffusion in the starting stage of the process flow combined with the following wafer thinning. Therefore, (i) it is not an n-type ***diffused*** layer, and moreover (ii) it is not an n-type ***residual*** diffused layer.

Employing an n-type residual diffused-layer as the buffer layer is one of the key points of the present invention. As noted in the application, when a high voltage is applied to a semiconductor switching device of the present invention,

> "the residual layer (of the priorly diffused n+ layer) contained in the n-type base can act as a field-stop layer due to its high doping concentration. Therefore, for the same voltage rating, the proposed structure can take a thinner n^- layer than without a stop layer, i.e. that of an NPT-IGBT. This would be notably advantageous in terms of on-voltage. Since the function of the highly-doped and concentration-graded residual layer is the same as that of the n^+ buffer layer in a PT-IGBT, the on-voltage of the proposed structure should be at the same and lowered level as that of a PT-IGBT. A stop-layer thickness of 25-50 μm is appropriate for a 2000 V device. If too thick, the on-stage will increase; if too thin, the field-stop function will be weakened which will result in a degraded breakdown voltage or an increased leakage current. On the other hand, this invention suggests **ultra-thin** and **lightly doped backside emitter with a thickness of less than 1 μm such that the electron current flowing through the backside emitter junction will be much larger than that in a PT-IGBT. Thus, the excess electrons stored in the n-type base can be easily drawn out through the backside emitter during the turn-off. It is in this way that the switching time is shortened.** Since this backside emitter is just the same as that of an NPT-IGBT, it can be predicted that this structure will be capable of the same shortened switching time as that of an NPT-IGBT."

Application, p. 6, line 21 through p. 7, line 7 (emphasis added). Thus, the n-type *residual diffused*-layer in the present invention performs a buffering role that allows for a thinner n- layer than would be possible without it. Thus, the *residual diffused* layer of the present invention is different from the prior art.

To understand the differences between the instant invention and the cited art, it would be useful to again consider the instant invention in the context of the prior art. As previously

mentioned in our Response to the Office Action of September 25, 2002, before the present application's priority date, i.e. before 2000, there were generally only two ways to produce IGBTs. One was the conventional PT-IGBT (punch-through type IGBT) (*See* IEDM Tech. Dig., pp. 264-267, 1982, and IEEE Trans. on Power Electronics, vol. PE-2, no. 3, (1987) pp. 194-207), which contains a very thick backside p+ emitter, an n+ buffer layer, an n- layer and a frontside structure formed on the topside of the n- layer. The process sequence of making the IGBT was as follows: starting with a p+ substrate, the n+ buffer layer and n- layer are formed by epitaxial growth, and the frontside structure was fabricated on the topside of the n- layer.

The second way to produce IGBTs was the NPT-IGBT technology firstly introduced by Siemens Co. (*See* IEEE PESC Record 1, pp. 21-25, 1989, and Proc. of ISPSD''96, pp. 331-334 and 169-172), where the starting substrate was an n- wafer instead of p+, and its frontside-structure was fabricated from the very beginning, followed by the thinning of the n- layer from the backside, and then the shallow p+ backside emitter was achieved by ion implantation.

There are several notable differences between the conventional PT- and the NPT-IGBTs. First, the fabricating sequence is very different as mentioned above. Second, in the PT-IGBT, there is an n+ buffer layer whereas in the NPT-IGBT there is no buffer layer. Thus, the n-layer of the NPT-IGBT must be thicker than that of the PT-IGBT to sustain the same high-voltage. With a buffer layer, the thickness of the n- layer can be reduced, and thereby the on-state voltage and excess carriers stored in the n- layer can be reduced (an advantage achieved by PT-IGBTs).

Third, generally speaking, the substrate must perform a mechanical sustaining function. Therefore, the p+ layer of the PT-IGBT is the thickest part in its structure. To reduce the series resistance, the p+ substrate of the PT-IGBT must be doped heavily. Compared with the thin and low-doped backside p+ emitter of the NPT-IGBT, the injection efficiencies of the more heavily doped p+ substrate of the PT-IGBT is high, relative to the NPT-IGBT. A lower injection efficiency means a larger electron current through the backside emitter junction, which can help the cleanup of excess carriers in the n- layer during the turn-off of the IGBT (an advantage was achieved by the NPT-IGBT technology). To further illustrate this point, the ion-implantation-formed, thin and low-

doped backside emitter of the NPT-IGBT is also referred to as ""transparent emitter (for electrons)"" or ""weak emitter"" (referring to US Patent 6,242,288 B1).

Fourth, since the injection efficiency of the PT-IGBT is high, an additional irradiation step must be combined to the fabricating sequence to reduce the lifetime of the carriers, which can help the cleanup of excess carriers in n- layer during turn-off and compensate the loss caused by the high injection efficiency.

Fifth, not using irradiation makes the temperature coefficient of the on-voltage of the NPT-IGBT positive, which is beneficial for parallel connection. By contrast, the temperature coefficient of the on-voltage of the PT-IGBT is negative due to its reduced carrier lifetime (*See* IEEE PESC 1989 Record 1, 1989, pp. 21 -25; Proc. ISPSD''97, 1997, pp. 237-240; and IEEE Trans. Ind. App., vol. 38, no. 1, pp. 168-174)

Sixth, the fabrication cost of the conventional PT is higher than that of the NPT especially for high-voltage IGBTs because the thick-layer epitaxial growth is expensive.

From the above discussion, it can be seen that both the conventional PT and the NPT technology possess their own drawbacks as well as their advantages.

The present invention, however, proposes a third way to produce a new kind of PT-IGBT. Please note that it is a NEW KIND of PT-IGBT, not the conventional PT-IGBT. This new kind of PT-IGBT combines the transparent backside emitter of the NPT and the buffer layer structure of the PT, which also combines the advantages achieved by them, i.e. a high electron current (being beneficial during turn-off), and a low on-voltage, less storage of excess carriers, respectively.

In the fabricating steps of this new kind of PT-IGBTs, the starting substrate is also an n- wafer just like that in NPT-IGBT technology and not like that in the conventional PT-IGBT. Firstly, a diffused, to be more accurate, a deeply-diffused (from near 100 to 200 microns or so) n+ layer is formed on the backside of the n+ substrate, the residual layer of which will act as a buffer layer in the future structure. Then, the frontside-structure is formed on the topside of the n+ substrate. And then the wafer subjects to a thinning from its backside to result in a residual layer of the previously diffused n+ layer to present a relatively thick and low-doped n-type buffer layer.

Finally, the p-type backside emitter is formed by ion implantation thus finishing the main phase of fabrication of the new PT-IGBT.

We use the residual of a diffused layer as the buffer layer for three reasons. (1) This method of introducing the buffer layer avoids the high-cost epitaxial growth of n+ buffer and n- layer for PT-IGBTs, and makes the whole process compatible to the low-cost fabricating process of the NPT. (2) A residual of a diffused layer can be controlled to be relatively thick (several microns to several tens of microns), and relatively low-doped, which can avoid remarkably affecting the injection efficiency of the backside emitter and overcome the drawbacks of FS IGBTs, whose idea is almost the same as the present invention but its method is not (*See* the specification of the present invention, pp. 2-3). (3) Not using a residual means a shallow diffusion (several microns to several tens of microns) must be carried out. Further, not using a residual means that we must use a thinner n- substrate, which tends to break during high-temperature processes because the difference of the substrate thicknesses for deep diffusion and shallow diffusion is of 100 microns or more.

From the above description, it is clear that the present invention is not obvious. The instant invention overcomes many problems to introduce a new generation of IGBT of low loss (both statically and dynamically). At the same time, this idea and its method can be easily applied to the domains of GTOs and MCTs, etc. To our knowledge, the method of the instant invention has not been duplicated or published in the prior art.

Having addressed the characterization of the admitted prior art in the Office Action, we can now turn to the cited reference. According to the Office Action,

> "Chang discloses (FIGS. 1-12 and related text) fabricating a frontside structure of an IGBT (col. 2, lines 5-11) on the low-concentration side of the n-type substrate 10 using ion implanting and high-temperature diffusion and thinning the wafer from the high-concentration side of the substrate by grinding and polishing so that the thickness of the residual diffused-layer is decreased to the range of approximately between 5 and 100 μm (col. 6, lines 9-28). Chang also discloses forming the backside p^+ emitter by ion implanting into the surface of the residual diffused-layer and depositing metals 104 on the surface of the backside p+ followed by sintering/alloying (col. 6, lines 29-44). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Chang to enable the residual diffused-layer of AAPA to be formed and

> furthermore to reduce the thickness of the substrate to the minimum necessary for electrical functioning of the transistors formed therein (Col. 6, lines 16-19).

See Office Action, pp. 4-5. However, Chang does not disclose a method in a form as stated by the Office Action.

First, in the Chang patent, the "substrate" for making the frontside structure is either composed of a monocrystalline n^+ substrate 10 and an n^- epitaxial layer 2 or just an n^--type substrate only. *See* Col. 4, lines 27-36. The Chang patent does not teach, suggest or disclose an n-type diffused layer.

Second, the Chang patent discloses grinding and polishing the backside surface of the monocrystalline substrate 10 during the wafer thinning process, not a n-type diffused layer. *See* Col. 6, lines 9-28. Thus, the resultant residual layer reserved or exposed by this treatment is not an n-type residual diffused-layer, but just a residual layer of the monocrystalline substrate 10. Thus, the Chang patent does not teach, suggest or disclose an n-type residual diffused-layer.

Finally, the Chang patent discloses backside p^+ implantation on the backside surface of the residual monocrystalline substrate 10, which is still not an n-type residual diffused layer. *See* Col. 6, lines 29-44). In fact, with a DMOSFET structure being formed on the frontside of the wafer, when there is no epi-layer 20 appearing, and the backside p^+ implantation occurs, the device structure can just be deemed as an NPT-IGBT. When an epi-layer 20 is present and the substrate 10 being n^+, the backside p^+ implantation is still not on a residual diffused-layer. While the epi-layer with the n^+ substrate may produce a kind of IGBT with an n^+ buffer layer, its thick epi-layer (especially for high-voltage IGBTs) will cause high costs, which is inferior to the instant invention where the epi-layer is avoided.

Finally, the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type residual diffused-layer recited in pending claims 2-5 and 7 are critical because they determine the injection efficiency of the backside emitter, which is very important for the low switching loss of the new PT-IGBT. And, to a large extent, the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type

residual diffused-layer also determine the thickness of n- layer for sustaining high-voltage, which is also very important for the low on-voltage and for switching loss. In fact, with this newly introduced buffer layer, controlling these parameters presents a NEW CHALLENGE for the semiconductor industry.

Although the claimed ranges of the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type residual diffused-layer may be optimal, they were first discovered and discussed in the instant invention. In summary, the instant invention teaches a method for manufacturing a new generation of IGBTs based on the idea of combining the PT structure and the transparent emitter. This combination is not obvious, but rather requires a deep understanding and perception of the prior art of IGBTs, a creative and careful design of the structure as departing from prior IGBT structures, and elaborate fabricating skills and capabilities.

Thus, none of the cited references teach, suggest or disclose the residual diffused layer of independent claim 6. Neither the admitted prior art nor the Chang patent (alone or in combination) teach, suggest, or disclose the method of the present invention.

Claims 2-5 depend from independent claim 6. As previously discussed, independent claim 6 is allowable over the cited art. For this reason, and for the independent distinctions described above, claims 2-5 are also allowable over the cited art. Reconsideration and notice to that effect is respectfully requested.

Thus, none of the cited references teach, suggest or disclose the residual diffused layer of the present invention. Neither the admitted prior art nor the Chang patent (alone or in combination) teach, suggest, or disclose the switching device or the method of the present invention. All of pending claims 1-6 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested.

With this Amendment, new claims 8-14 are added. Independent claim 9 requires "a residual diffused layer", an element that is not disclosed, taught or suggested by the cited art. Claims 10-14 depend from claim 9. All of pending claims 8-14 are allowable over the cited references for the same reasons as presented above with respect to claims 1-6.

With this amendment, all of pending claims 1-6 and 8-14 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested. The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

Respectfully submitted,

KINNEY & LANGE, P.A.

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